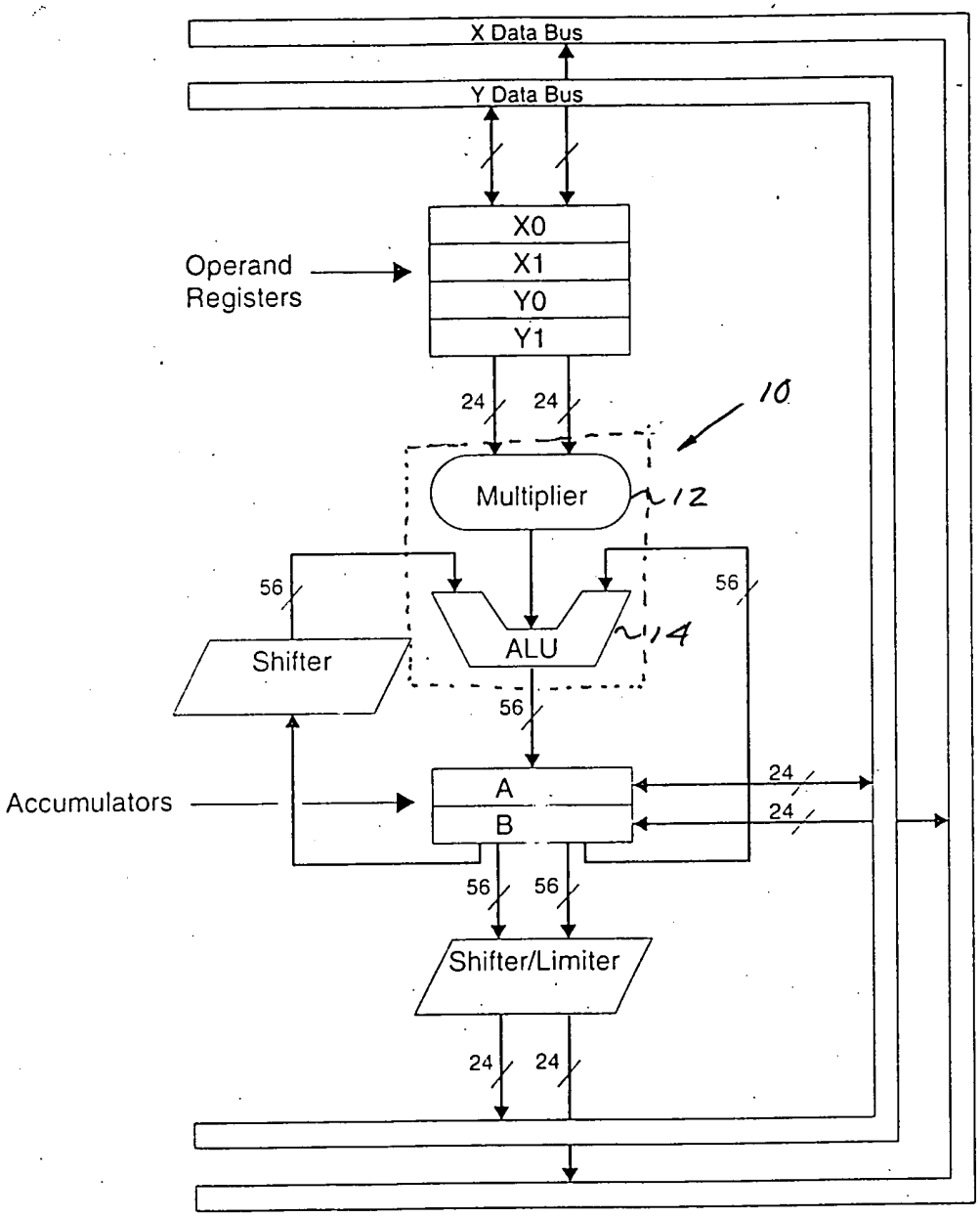
FIG. 1 (PRIOR ART)



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DOCKET" 22822560

FIG. 2 (PRIOR ART)

	INSTRUCTION CYCLE								
	1	2	3	4	5	6	7	8	...
INST. FETCH	B	I	–	–	X_1	X_2	X_3	X_4	...
DECODE		B	–	–	–	X_1	X_2	X_3	...
DATA R/W			B	–	–		X_1	X_2	...
EXECUTE				B	NOP	NOP	NOP	X_1	...

Fig. 3

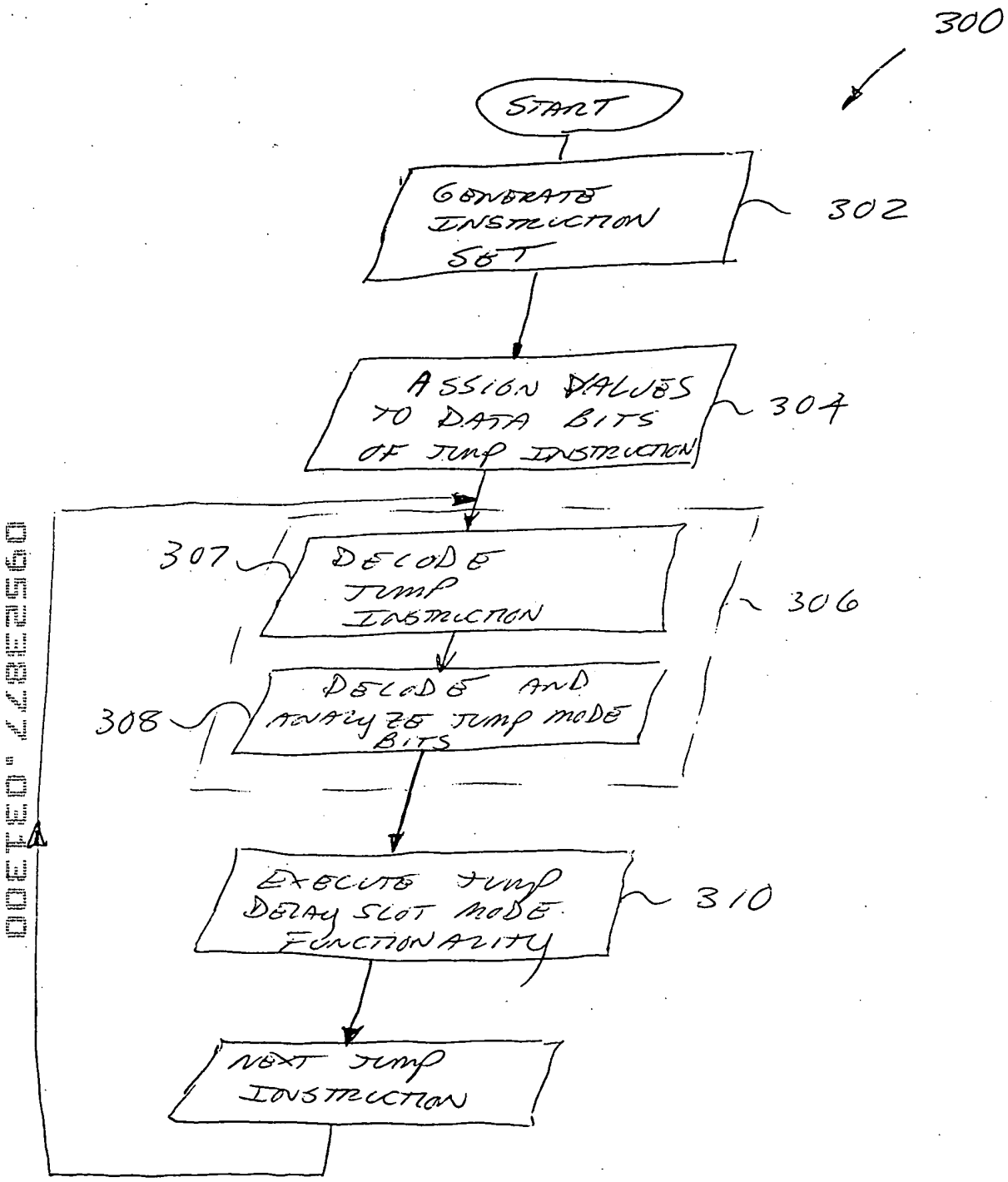
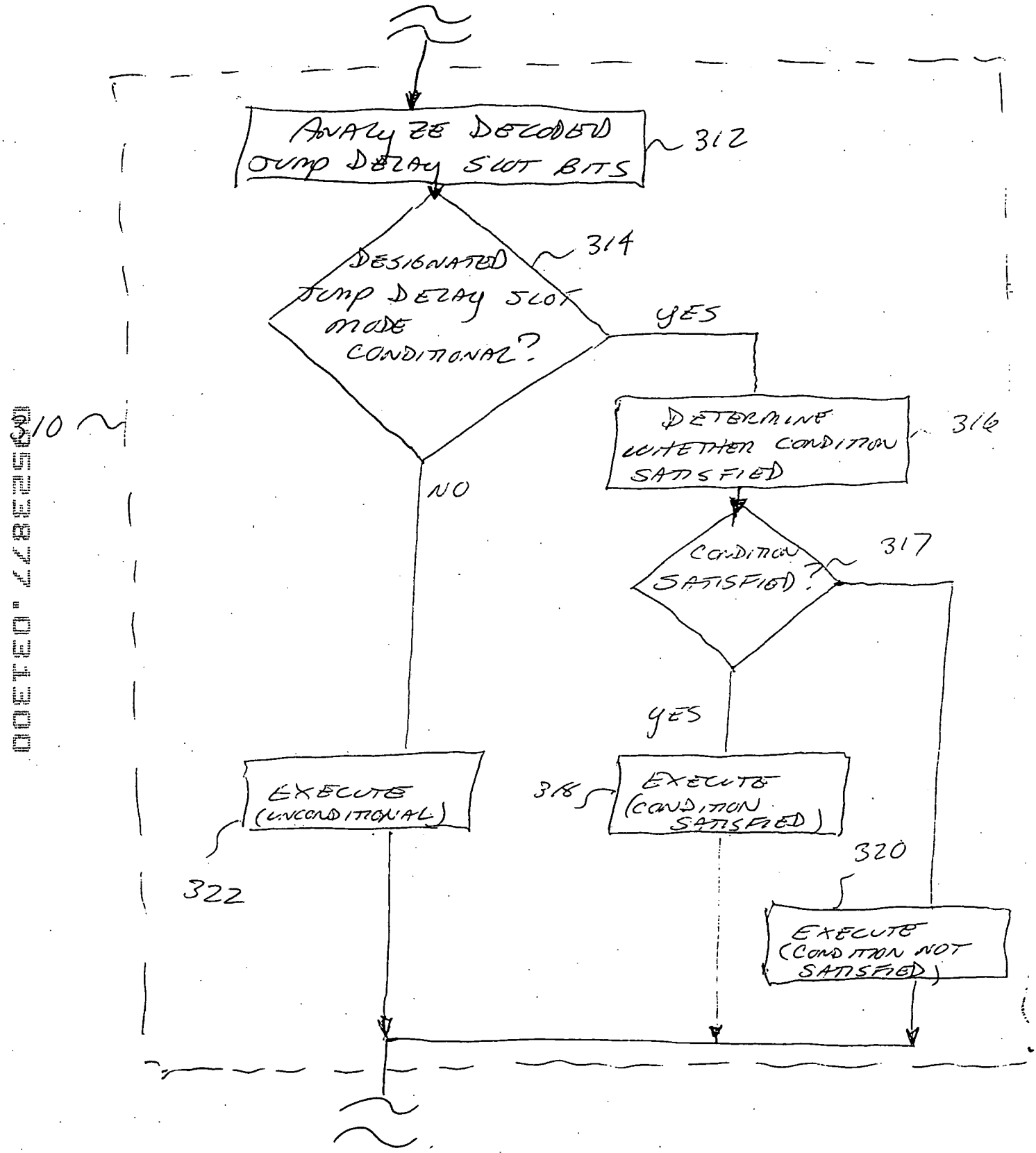

300
START
GENERATE INSTRUCTION SET
302
ASSIGN VALUES TO DATA BITS OF JUMP INSTRUCTION
304
306
307
DECODE JUMP INSTRUCTION
308
DECODE AND ANALYZE JUMP MODE BITS
310
EXECUTE JUMP DELAY SLOT MODE FUNCTIONALITY
NEXT JUMP INSTRUCTION
A
0054.0 / 2.3.2.5.5.0

FIG. 3a


ANALYZE DECODED JUMP DELAY SLOT BITS
312
DESIGNATED JUMP DELAY SLOT MODE CONDITIONAL?
314
YES
NO
DETERMINE WHETHER CONDITION SATISFIED
316
CONDITION SATISFIED?
317
YES
EXECUTE (UNCONDITIONAL)
322
EXECUTE (CONDITION SATISFIED)
318
EXECUTE (CONDITION NOT SATISFIED)
320
310

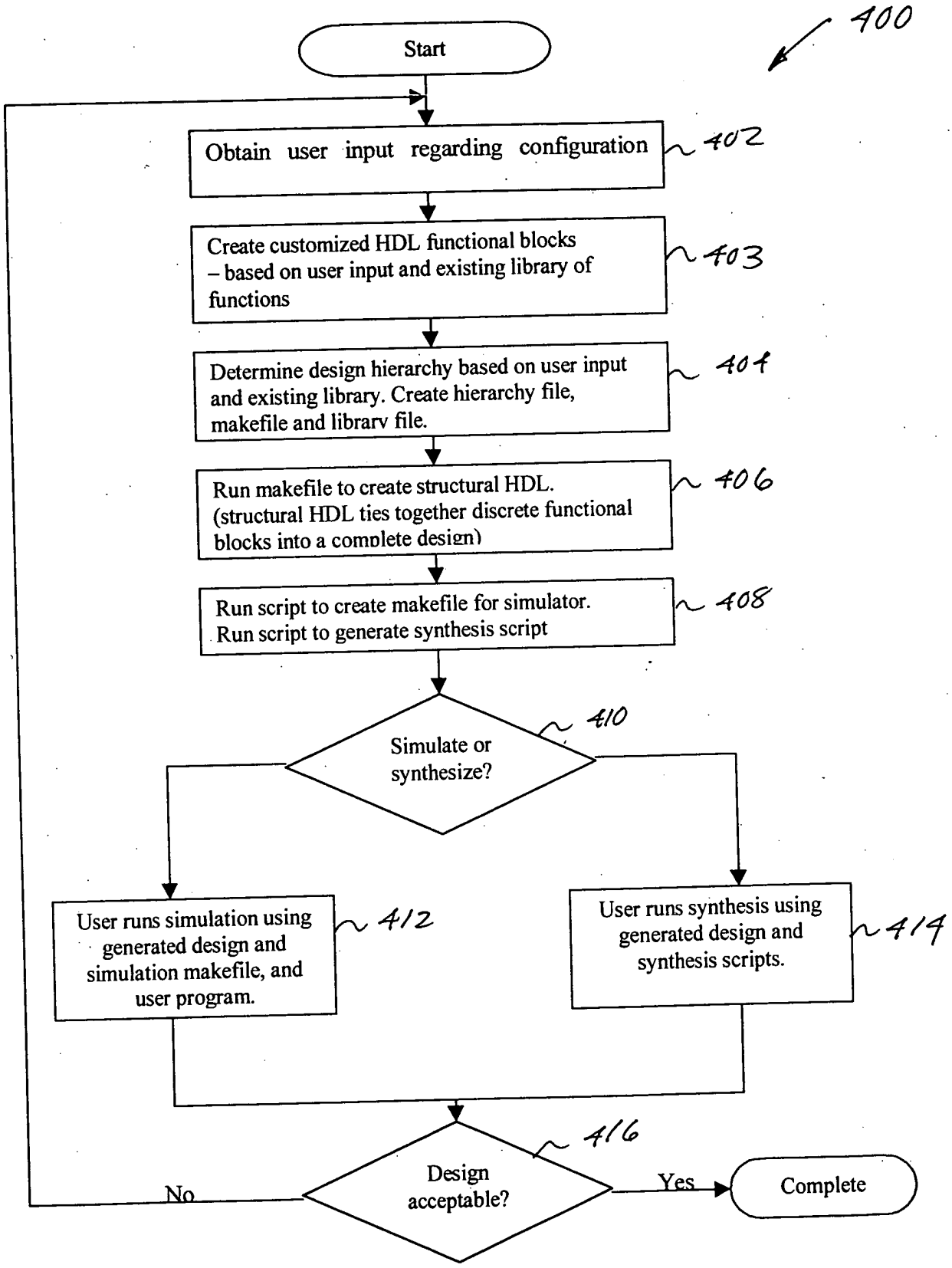
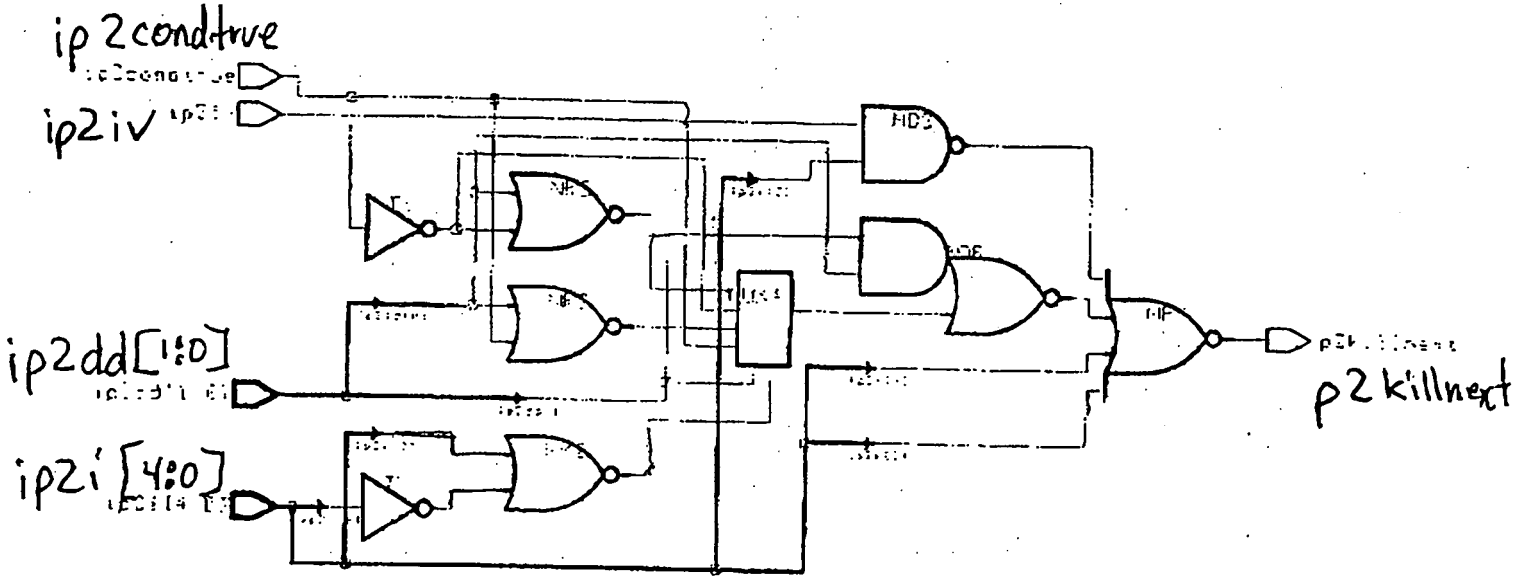


FIG. 4

09539897 - 050300

00ETE0' 27BE2560

5 -Unconstrained delay slot cancelling logic

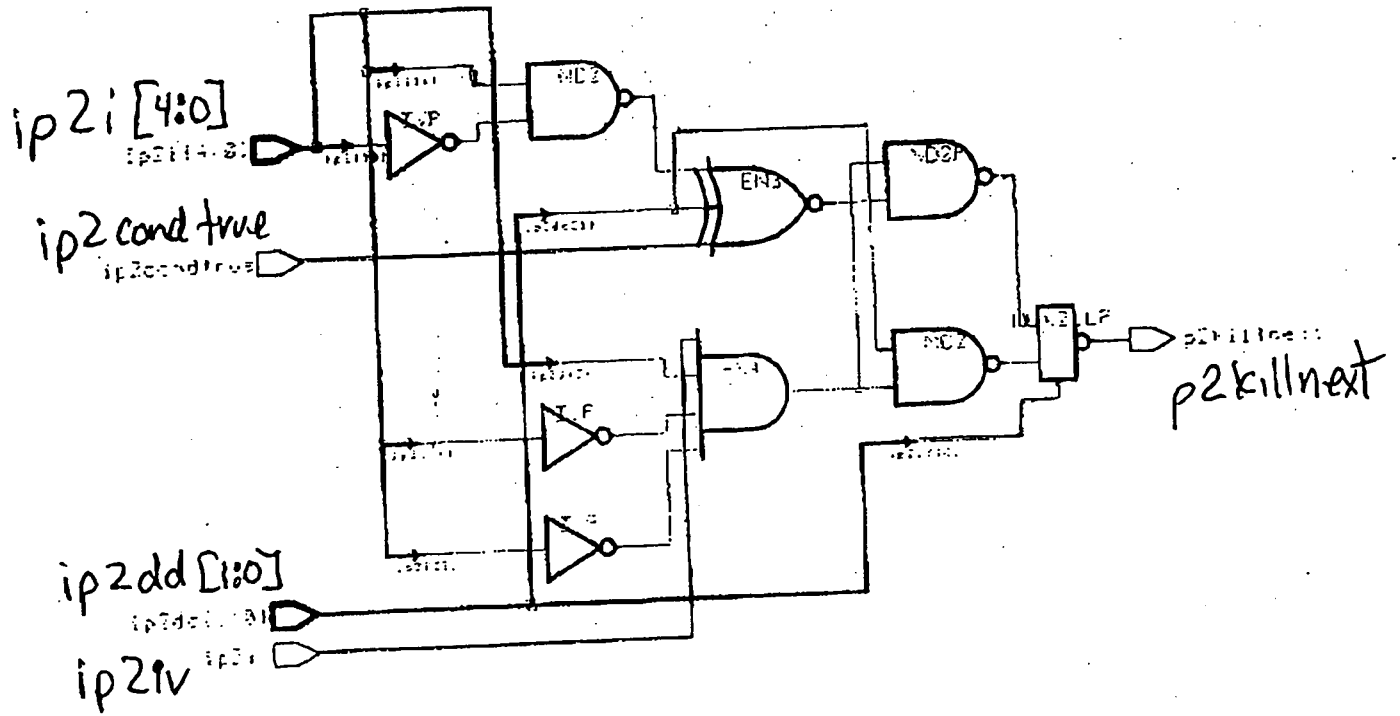


design: dela_slot	designer: James Harevill	date: 5/13/99
technolog.: lsi_10k	company: IPC Cores Ltd	sheet 1 of 1

FIG. 5

00E60 "278E2560

6 Constrained delay slot cancelling logic



design: dela_slot	designer: James Hakewill	date: 9/3/99
technology: tsi_10k	company: ARC Cores Ltd.	sheet: 1 of 1

FIG. 6

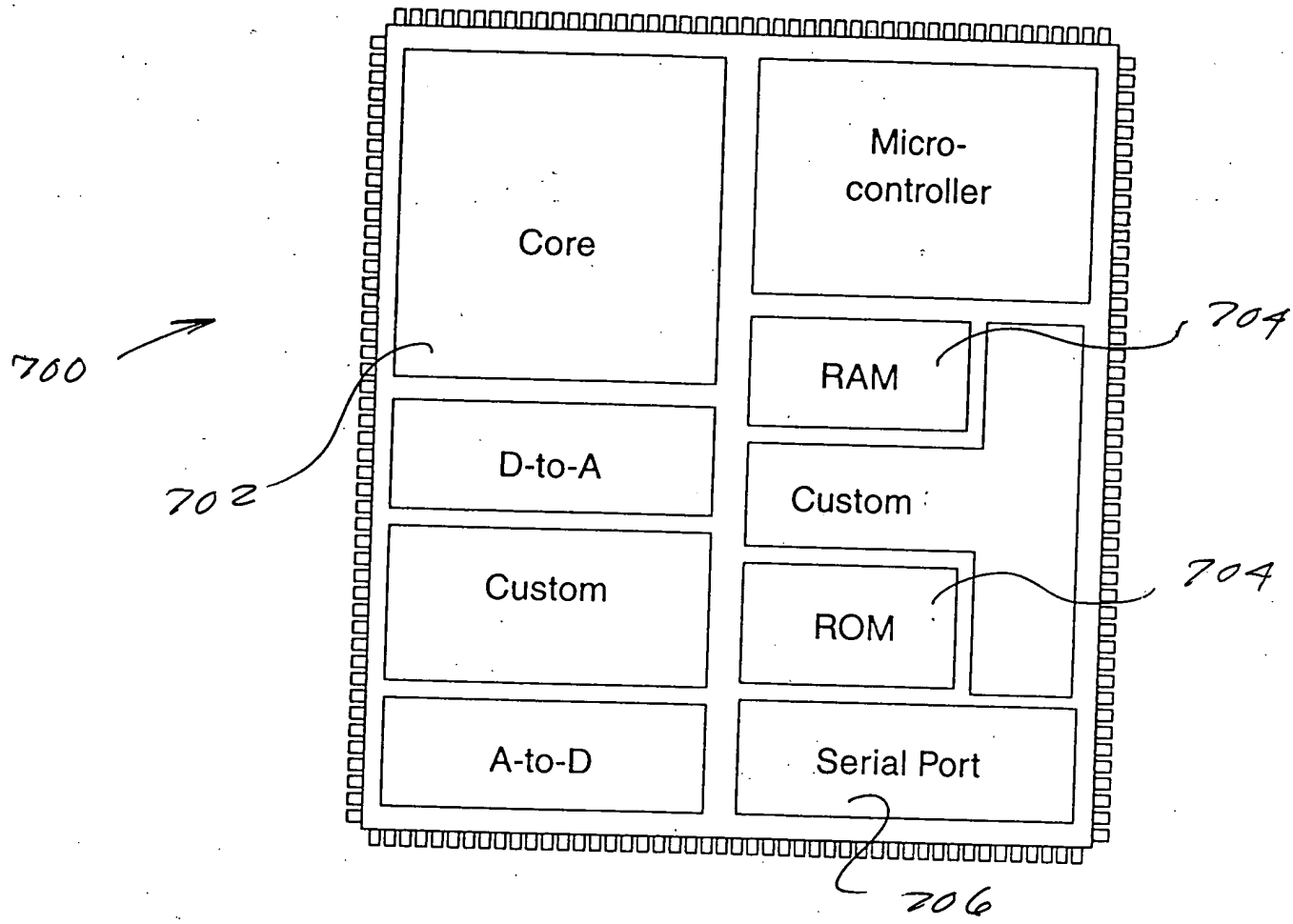


FIG. 7

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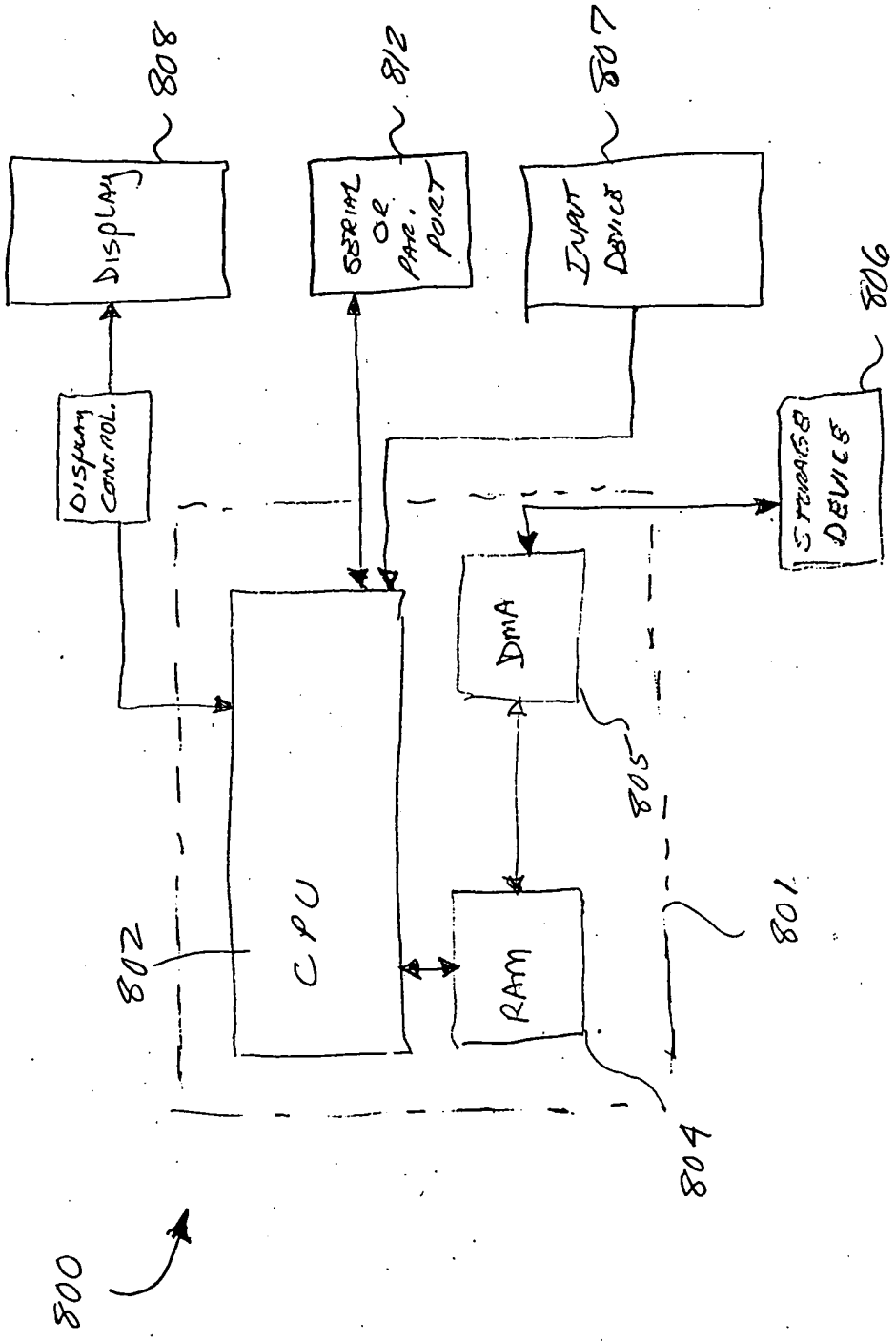

FIG. 8

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